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| KERALA TECHNOLOGICAL UNIVERSITY  http://ktu.edu.in/images/logo_final.png  **SCHEME AND SYLLABUS**  **FOR**  **M. Tech. DEGREE PROGRAMME**  **IN**  **ELECTRONICS AND COMMUNICATION ENGINEERING**  **WITH SPECIALIZATION**  **VLSI AND EMBEDDED SYSTEMS**  **CLUSTER 05 (ERNAKULAM II)**  **KERALA TECHNOLOGICAL UNIVERSITY CET Campus, Thiruvananthapuram Kerala, India -695016**  **(2015 ADMISSION ONWARDS)** |

**KERALA TECHNOLOGICAL UNIVERSITY**

**SCHEME AND SYLLABUS FOR M. Tech. DEGREE PROGRAMME**

**Branch: ELECTRONICS AND COMMUNICATION ENGINEERING**

**Specialization: VLSI AND EMBEDDED SYSTEMS**

**SEMESTER – I**

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| ***Exam Slot*** | ***Course No*** | ***Subjects*** | *L-T-P* | *Internal Marks* | *End Semester Exam* | | *Credits* |
| Marks | Duration  (hrs) |
| A | 05EC 6001 | CMOS Analog Design | 3-1-0 | 40 | 60 | 3 | 4 |
| B | 05EC 6003 | CMOS Digital Design | 3-1-0 | 40 | 60 | 3 | 4 |
| C | 05EC 6005 | Advanced Digital Design | 3-1-0 | 40 | 60 | 3 | 4 |
| D | 05EC 6007 | Embedded Processors | 2-1-0 | 40 | 60 | 3 | 3 |
| E | 05EC 601x | Elective 1 | 2-1-0 | 40 | 60 | 3 | 3 |
|  | 05EC 6077 | Research methodology | 1-1-0 | 100 | 0 | 0 | 2 |
|  | 05EC 6091 | HDL Lab | 0-0-2 | 100 | 0 | 0 | 1 |

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| **Elective – I** | |
| **Course No** | **Subjects** |
| 05EC 6011 | FPGA Based System Design |
| 05EC6013 | Modelling of Embedded Systems |
| 05EC 6015 | Semiconductor Device Physics and Modelling |

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**SEMESTER – II**

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| ***Exam Slot*** | ***Course No*** | ***Subjects*** | ***L-T-P*** | ***Internal Marks*** | ***End Semester Exam*** | | ***Credits*** |
| Marks | Duration (hrs) |
| A | 05EC 6002 | Mixed Signal VLSI Design | 3-1-0 | 40 | 60 | 3 | 4 |
| B | 05EC 6004 | Sensor Technologies and MEMS | 2-1-0 | 40 | 60 | 3 | 3 |
| C | 05EC 6006 | Embedded Real Time Systems | 2-1-0 | 40 | 60 | 3 | 3 |
| D | 05EC 602x | Elective 2 | 2-1-0 | 40 | 60 | 3 | 3 |
| E | 05EC 603x | Elective 3 | 2-1-0 | 40 | 60 | 3 | 3 |
|  | 05EC 6066 | Seminar - I | 0-0-2 | 100 | 0 | 0 | 2 |
|  | 05EC 6088 | Mini Project | 0-0-4 | 100 | 0 | 0 | 2 |
|  | 05EC 6092 | Embedded Systems Lab | 0-0-2 | 100 | 0 | 0 | 1 |

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| **Elective – II** | |
| **Course No** | **Subjects** |
| 05EC 6022 | Design of Power Converters |
| 05EC 6024 | System Identification and System Simulation |
| 05EC 6026 | VLSI Process Technology |

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| **Elective – III** | |
| **Course No** | **Subjects** |
| 05EC 6032 | High Speed Digital Design |
| 05EC 6034 | Low Power VLSI Design |
| 05EC 6036 | Nanomaterials, Structures and Devices |

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**SEMESTER – III**

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| ***Exam Slot*** | ***Course No*** | ***Subjects*** | ***L-T-P*** | ***Internal Marks*** | ***End Semester Exam*** | | ***Credits*** |
| Marks | Duration(hrs) |
| A | 05EC704x | Elective 4 | 2-1-0 | 40 | 60 | 3 | 3 |
| B | 05EC705x | Elective 5 | 2-1-0 | 40 | 60 | 3 | 3 |
|  | 05EC7067 | Seminar II | 0-0-2 | 100 | 0 | 0 | 2 |
|  | 05EC7087 | Project (Phase 1) | 0-0-12 | 50 | 0 | 0 | 6 |

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| **Elective – IV** | |
| **Course No** | **Subjects** |
| 05EC7041 | Electromagnetic Compatibility |
| 05EC7043 | Testing of VLSI Circuits |
| 05EC7045 | VLSI Signal Processing |
| **Elective – V** | |
| **Course No** | **Subjects** |
| 05EC7051 | VLSI and Computer Aided Design |
| 05EC7053 | Hardware / Software Co-design |
| 05EC7055 | Embedded Networking |

**SEMESTER – IV**

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| **Exam**  **Slot** | **Course**  **No** | **Subjects** | **L-T-P** | **Internal**  **Marks** | **End Semester Exam** | | | **Credits** |
| **Marks** | | **Duration(hrs)** |
|  | 05EC7088 | Project(Phase 2) | 0-0-21 | 70 | 30 | - | | 12 |

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Total:68

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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 6001** | | CMOS ANALOG DESIGN | 3-1-0-4 | 2015 | |
| COURSE OBJECTIVES:   * To analyse and design MOS sub circuits like current mirrors and references. * To analyse MOS single stage amplifiers and differential amplifiers. * To provide knowledge about MOS operational amplifier. * To study the frequency response of MOS Single-Stage Amplifiers, Differential Pairs and Operational Amplifiers and to understand the effect of noise in different analog circuits.   **COURSE OUTCOMES:**   * Students can design and analyze current mirrors, references and different MOS amplifiers. * Students are able to design CMOS based operational amplifier for the given specification. * Students will in a position to analyse CMOS based Analog circuits and the effect of noise in it.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (36 hrs) | | | | HRS |
| **I** | Analog Sub-circuits: MOS Switch, Active Resistor, Current Sinks and Sources. Current Mirrors: Simple Current Mirror, Cascode Current Mirror, Wilson Current Mirror. Cascode configurations: Telescopic, Folded. Voltage References: Supply Independent Biasing, Temperature Independent References, Band-Gap Referenced Circuit. | | | | 9 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | Single stage amplifiers: MOS Single Stage Amplifiers: CS, CG, CD, Differential amplifier (all with resistive and active loads). | | | | 9 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | Operational Amplifiers: Single Stage Op Amps, Two-Stage Op Amps, Cascode and folded cascode Op- amps, Transconductance Amplifier. | | | | 10 |
| **IV** | Frequency Response: Miller Effect, Association of Poles with Nodes, Phase Margin, Frequency Compensation, Frequency Response of Single-Stage Amplifiers, Differential Pairs, Operational Amplifiers. Noise: Types Of Noise, Representation of Noise in Circuits, Noise in Single-Stage Amplifiers, Differential Pairs, Operational Amplifiers, Noise Bandwidth product. | | | | 8 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. R. Jacob Baker, Harry W Li, David E Boyce, “CMOS – Circuit Design, Layout, and Simulation”, 3rd Edition, 1998. 2. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Tata McGraw Hill, 2008. 3. Gray, Hurst, Lewis, Meyer, “Analysis and Design of Analog Integrated Circuits”, 5th Edition, Wiely India, 2010. 4. Philip E Allen, Douglas R Holberg, “CMOS Analog Circuit Design”, International Student(Second) Edition, 2010. | | | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 6003** | | CMOS DIGITAL DESIGN | 3-1-0-4 | 2015 | |
| COURSE OBJECTIVES:   * To study advanced concepts of CMOS Digital Design. * To cover crucial real world system design issues such as signal integrity, power dissipation, interconnect packaging, timing and synchronization. * To provide unique coverage of the static and dynamic circuits. * To get the idea of designing arithmetic and logic circuits and memory elements.   **COURSE OUTCOMES:**   * Students can model and estimate R, L, and C parasitics, effect of technology scaling, techniques to cope with ohmic drop and capacitive cross talk, estimate RC delay, and inductive effects. * Students can design arithmetic and logic circuits and memory elements**.**   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (36 hrs) | | | | HRS |
| **I** | Introduction to CMOS technology: MOS Transistors, CMOS logic, CMOS fabrication and Layout, Design partitioning, Circuit design, Physical design, Design verification, Fabrication, Packaging and testing. Static CMOS Inverter: DC Characteristics, Beta Ratio Effects, Noise Margin, Pass Transistor DC Characteristics. Delay Models: Introduction, Definitions, Timing Optimization. RC Delay Model: Effective Resistance, Gate and Diffusion Capacitance, Equivalent RC Circuits, Elmore Delay, Layout Dependence of Capacitance, Determining Effective Resistance. Linear Delay Model: Logical Effort, Parasitic Delay, Delay in a Logic Gate, Limitations to the Linear Delay Model. Logical Effort of Paths: Delay in Multistage Logic Networks, Choosing the Best Number of Stages, Example, Limitations of Logical Effort, Iterative Solutions for Sizing. | | | | 9 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | Interconnect effects and power analysis: Introduction, Wire Geometry, Interconnect Modelling: Resistance, Capacitance, Inductance. Interconnect Impact: Delay, Energy, Crosstalk, Inductive Effects, Effective Resistance and Elmore Delay. Power: Sources of Power Dissipation, Dynamic Power, Static Power, On-Chip Power Distribution Network. On-Chip Bypass Capacitance, Power Network Modelling , Power Supply Filtering, Charge Pumps. Energy Scavenging. Clocks: Clock System Architecture, Global Clock Generation, Global Clock Distribution, Local Clock Gaters, Clock Skew Budgets, Adaptive Deskewing, PLLs and DLLs. I/O: Basic I/O Pad Circuits, Electrostatic Discharge Protection. | | | | 9 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | Static and Dynamic circuits: CMOS Inverter: tristate inverter, Other static CMOS logic gates, static properties (2 input NAND, NOR), Combinational logic circuits. Layout-examples. Fundamentals of dynamic logic:, Dynamic pass transistor circuits, CMOS circuits, High performance dynamic circuits-Domino CMOS, Multi Output Domino Logic, Dual-rail Domino Logic, NP Domino logic (NORA), True-Single-Phase-Clock(TSPC) CMOS logic. BiCMOS logic gates. Silicon-On-Insulator Circuit Design: Floating Body Voltage, SOI Advantages, Disadvantages. Introduction to network on chip(NOC). Sequential Circuit Design: Sequencing Static Circuits, Sequencing Methods, Max-Delay Constraints, Min-Delay Constraints, Time Borrowing, Clock Skew. | | | | 9 |
| **IV** | Designing arithmetic building blocks: Adders: Design considerations, Fast adders, Multipliers: Unsigned Array Multiplication, Two's Complement Array Multiplication, Booth Encoding, Column Addition, Final Addition, Fused Multiply-Add, Shifters: Funnel shifter, Barrel shifter. Designing of memory and array structures: SRAM: SRAM Cells, Row Circuitry, Column Circuitry. Area, Delay and Power of RAMs. DRAM: Subarray Architectures, Column Circuitry, Embedded DRAM. Read-Only Memory: Programmable ROMs, NAND ROMs, Flash Serial Access Memories: Shift Registers, Queues (FIFO, LIFO), Content-Addressable Memory: Programmable Logic Arrays. | | | | 9 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. Weste and Harris, “Integrated Circuit Design”, 4/e, 2011, Pearson Education**.** 2. Sung-Mo Kang, Yusuf Leblebici, “CMOS Digital Integrated Circuits, 3/e, Tata McGraw-Hill Education, 2003. 3. Rabaey, Chandrakasan and Nikolic, “Digital Integrated Circuits – A Design Perspective”, 2/e, Pearson Education. 4. R. Jacob Baker, Harry W. Li, David E. Boyce, “CMOS, Circuit Design, Layout, and Simulation”, 3/e, Wiley Interscience. | | | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 6005** | | ADVANCED DIGITAL DESIGN | 3-1-0-4 | 2015 | |
| COURSE OBJECTIVES:   * The student will learn the analysis and synthesis of combinational and sequential circuits. * Learn the principles of digital design and practices using data path components such as counters, shift registers, and adders etc. * To introduce Register Transfer Level (RTL) design. * The student will learn about optimizations and trade-offs in combinational logic, sequential logic, data path component and RTL design.   **COURSE OUTCOMES:**   * Ability to design and implement various optimized combinational and sequential digital circuits.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (36hrs) | | | | HRS |
| **I** | Combinational Logic: Switching Algebra. Combinational-Circuit Analysis. Combinational- Circuit Synthesis. Programmed Minimization Methods. Timing Hazards, Sequential Logic Design: Latches, flip flops, timing, and glitches, Finite State Machines: analysis, State diagrams and ASM charts, Transition Lists. Decomposing State Machines. Feedback Sequential Circuits. Feedback Sequential Circuit Design. | | | | 9 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | Combinational and Sequential-Circuit Documentation Standards. Datapath Design: Datapath Components: Registers, Adder, Comparators, Multiplier—Array-Style, Subtractors and Signed Number, Arithmetic-Logic Units—ALUs, Shifters, Counters and Timers, Register Files. Synchronous Design Methodology, Iterative versus Sequential Circuits Impediments to Synchronous Design. Synchronizer Failure and Metastability. Controller Design and Implementation: Random Logic, Time State (Divide and Conquer), Jump Counter, Branch Sequencers, Microprogramming, Control parallelism, pipelining. | | | | 9 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | Register-Transfer Level (RTL) Design: High-Level State Machine, RTL Design Process, Determining Clock Frequency, Behavioural-Level Design: C to Gates, Memory Components, Queues, FIFOs, Multiple Processors, Hierarchy-A Key Design Concept. | | | | 9 |
| **IV** | Optimizations and Tradeoffs: Combinational Logic Optimizations and Tradeoffs, Sequential Logic Optimizations and Tradeoffs, Data path Component Tradeoffs, RTL Design Optimizations and Tradeoffs, Tradeoffs in Design: A case study. | | | | 9 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. Frank Vahid, “Digital Design with RTL Design, VHDL and Verilog”, 2/e, Wiley, 2010. 2. Harris & Harris, “Digital Design and Computer Architecture”, 2/e, Morgan Kaufmann, 2012. 3. John F. Wakerly, “Digital Design Principles and Practices”, 4/e, Prentice Hall, 2005. 4. William James Dally, R. Curtis Harting, “Digital Design: A Systems Approach”, Cambridge University Press, 2012. 5. Randy H. Katz and Gaetano Borriello , “Contemporary Logic Design”, 2/E, Prentice Hall India, 2009. | | | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 6007** | | EMBEDDED PROCESSORS | 2-1-0-3 | 2015 | |
| COURSE OBJECTIVES:   * Introduce the basics of Advanced Microcontrollers and DSP processors. * Introduce TMS320F28335 digital signal Processor, functional blocks and peripherals. * To implement DSP functions in a DSP platform. * To introduce functional blocks of ARM microcontroller and its peripherals. * To expose the students with different tools for development, testing and debugging of Microcontrollers and DSP Processors.   **COURSE OUTCOMES:**   * Students will be able to design embedded systems using ARM processor and DSP processor. * The students will be able to select hardware and software components for optimized performance. * The students will have knowledge regarding networking components and sensors along with their applications.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (27hrs) | | | | HRS |
| **I** | Digital Signal Processors- TMS320F28335 digital signal Processor, functional overview, Memory Mapping, fetch and execute, pipelining, Linear and circular addressing modes, Memory bus, peripheral bus, Oscillator, PLL and clocking mechanisms, interrupts. DSP Peripherals: Direct Memory Access (DMA), CPU-Timers, PWM modules, enhanced capture modules, QEP modules, analog-to-digital converter (ADC) module, controller area network modules, serial communications interface modules, serial peripheral interface (SPI) module, Inter-integrated circuit module (I2C), Digital I/O and shared pin functions. | | | | 7 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | Filter design in DSP processor: Introduction to z-transform, Mapping from s-Plane to z-Plane, Difference Equations, Discrete Signals, Finite Impulse Response (FIR) Filters, FIR Implementation Using Fourier Series, Lowpass FIR Filter, Window Functions, Computer-Aided Approximation, Programming Examples Using C and ASM code, FIR Filter Implementation: Band-stop and Band-pass. | | | | 7 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | ARM Processor Architecture: Functional block Diagram, RISC advantage, Register set, Pipeline, Exceptions & Interrupts, Memory mapping control. ARM Peripherals access: Crystal oscillator, PLL, reset and wakeup timer, Timers, Event counters, Interrupt, ADC, DAC. Communication protocols: Ethernet, USB, CAN, SPI, I2C, PWM. | | | | 7 |
| **IV** | Architectural support for high level languages-Data types, Floating point data types, Conditional statements, Loops, Use of memory, Run-time environment, Programmer`s model, Development tools. Architectural support for system development- ARM memory interface, AMBA, ARM reference peripheral specifications, h/w system prototyping tools, ARM emulator, JTAG, ARM debug architecture, Embedded trace, signal processing support. | | | | 6 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. Rulph Chassaing, “DSP Applications Using C and the TMS320C6x DSK”, RulphChassaing, John Wiley & Sons Inc, 2002. 2. Robert Oshana, “DSP Software Development Techniques for Embedded and Real-Time Systems”, Newnes, 2006. 3. Steve Furber, "ARM System-on-chip architecture", Pearson Education. 4. Wayne Wolf, "Computers as Components-principles of Embedded computer system design", Elseveir. 5. Andrew N Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide", Elseveir. 6. David E. Simon, "An Embedded Software Primer", Pearson Education. 7. TMS320F28335 datasheet. 8. LPC1769 datasheet.   **WEB:**  1. www.ti.com | | | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 6011** | | FPGA BASED SYSTEM DESIGN (ELECTIVE 1) | 2-1-0-3 | 2015 | |
| COURSE OBJECTIVES:   * To illustrate the basic concepts of FPGA based digital design. * To design synthesizable digital sub-system components using Verilog HDL.   **COURSE OUTCOMES:**  Upon successful completion of this course, students will be able to:   * Design and optimize complex combinational and sequential circuits. * Design and model digital circuits with Verilog HDL at behavioural, structural and RTL Levels. * Develop test benches to simulate combinational and sequential circuits.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (27hrs) | | | | HRS |
| **I** | Verilog HDL-based design, Gate-level combinational circuit, Basic lexical elements and data types, Overview of FPGA and EDA software, RT-level combinational circuit, Operators, Always block, Conditional statements, Parameter and constant, Sequential Circuit, HDL code of Flip-Flop and register, Test bench, Design examples. | | | | 7 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | FSM, Mealy and Moore outputs, FSMD, ASMD chart, Code development, Blocking and non-blocking assignments, signed data types, functions, Constructs for test bench development, Design examples. | | | | 7 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | I/O Modules: UART receiving subsystem, UART transmitting subsystem, UART verification, HDL implementation, Design of Full-featured UART, automatic baud rate detection circuit, UART-controlled stopwatch, UART-controlled rotating LED banner, External SRAM, IS61LV25616AL SRAM, Block diagram and I/O signals, memory controller, Design, Timing analysis, HDL implementation, SRAM testing circuit. Xilinx Spartan3 Specific Memory, Methods to incorporate memory modules, HDL templates for memory inference. | | | | 7 |
| **IV** | I/O Modules, Graphics mode VGA controller, VGA synchronization, Timing calculation, HDL implementation, Graphic generation with an object-mapped scheme, Graphic generation with bit-mapped scheme, Text mode VGA controller, Text generation, Font ROM, Font scaling, HDL implementation. Mini project based on suggested experiments given in reference. Simulation and experimental verification is mandatory. | | | | 6 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. Pong P. Chu, "FPGA Prototyping by Verilog Examples", John Wiley & Sons, 2008 2. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Second Edition, Prentice Hall PTR, 2003 3. Zainalabedin Navabi, "Digital Design and Implementation with Field Programmable Devices", Springer, 2004 4. B. Bala Tripura Sundari, T. R. Padmanabhan, "Design Through Verilog HDL", Wiley India, 2012 | | | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 6013** | | MODELLING OF EMBEDDED SYSTEMS(ELECTIVE 1) | 2-1-0-3 | 2015 | |
| COURSE OBJECTIVES:   * Standard system design methodologies. * Modelling of hardware and software components. * Software and hardware synthesis, functional connectivity and sharing. * System startup methods, boot up codes. * Tools for design of software and hardware, simulation and verification.   **COURSE OUTCOMES:**   * The students will have systematic approach towards the embedded system design.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (27hrs) | | | | HRS |
| **I** | Introduction, System Design Methodologies & Models: - System-Design Challenges Abstraction Levels, System Design Methodology, and System-Level Models PlatformDesign System Design Tools. System Design Methodologies- Bottom-up Methodology, Top-down Methodology, Meet-in-the-middle Methodology Platform Methodology Field Programmable Gate Array (FPGA) Methodology System-level Synthesis Processor Synthesis. Models-Models of Computation, System Design Languages, System Modelling, Processor Modelling, Communication Modelling, System Models. | | | | 7 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | System Synthesis:-System Design Trends, Transaction Level Model(TLM) Based Design, Automatic TLM Generation, Automatic Mapping Platform Synthesis, Software synthesis- Preliminaries, Software Synthesis Overview, Code Generation, Multi-Task Synthesis, Internal Communication, External Communication, Startup Code, Binary Image Generation Execution. | | | | 7 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | Hardware synthesis:- Register Transfer Logic(RTL) Architecture, Input Models Estimation and Optimization, Register Sharing, Functional Unit Sharing, Connection Sharing, Register Merging, Chaining and Multi-Cycling, Functional-Unit Pipelining, Datapath Pipelining, Control and Datapath Pipelining, Scheduling Interface Synthesis. | | | | 7 |
| **IV** | Verification: - Simulation Based Methods, Formal Verification Methods, Comparative Analysis of Verification Methods, System Level Verification. Embedded Design Practise -System Level Design Tools, Embedded Software Design Tools, Hardware Design Tools, Case Study. | | | | 6 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. Daniel D. Gajski , Samar Abdi Andreas and Gerstlauer Gunar Schirner , “Embedded System Design Modelling , Synthesis & Verification”, Springer, 2009. 2. A. Jantsch, Morgan , “Modelling Embedded Systems and SoCs - Concurrency and Time in Models of Computation”, Kaufmann, 2003. 3. Gomaa , “Software Design Methods for Concurrent and Real-time Systems”, Addison-Wesley, 1993. 4. Henzinger, T., Sifakis J, "The Discipline of Embedded System Design". 5. Frank Vahid and Tony D. Givargis, "Embedded System Design: A Unified Hardware/Software Introduction", 2000. 6. Wayne Wolf, "Computers as Components-principles of Embedded computer system design", Elseveir, 2005. 7. J. Banks, J. S. Carson II, B. L. Nelson, and D. M. Nicol, "Discrete-Event System Simulation", Prentice-Hall, 2001. | | | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 6015** | | SEMICONDUCTOR DEVICE PHYSICS AND MODELLING (ELECTIVE 1) | 2-1-0-3 | 2015 | |
| COURSE OBJECTIVES:   * To analyse the advanced concepts of semiconductor device modelling. * To understand how devices and integrated circuits are fabricated. * To discuss modern trends in the microelectronics industry.   **COURSE OUTCOMES:**   * Upon successful completion of this course, students will be able to apply concepts of semiconductor device physics and principles to the microelectronics industry.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (27hrs) | | | | HRS |
| **I** | Semiconductors Fundamentals, Mosfet Overview and MOS Capacitor: Semiconductors: Intrinsic Semiconductors, Free Electrons, and Holes, Extrinsic Semiconductors, Equilibrium in the Absence of Electric Field, Equilibrium in the Presence of Electric Field, Nonequilibrium; Quasi-Fermi Levels, Relations between Charge Density, Electric Field, and Potentials; Poisson's Equation. Conduction: Transit Time, Drift, Diffusion, Total Current. Contact Potentials, The pn Junction: Overview of the MOS Transistor: Basic Structure, A Qualitative Description of MOS Transistor Operation, MOS Transistor Characteristics. The Mos Capacitor: The Flatband Voltage, Potential Balance and Charge Balance, Effect of Gate-Body Voltage on Surface Condition: Flatband Condition, Accumulation, Depletion, Analysis, Inversion: General Relations and Regions of Inversion, Strong Inversion, Weak Inversion, Moderate Inversion. | | | | 7 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | The Three-Terminal Mos Structure: Contacting the Inversion Layer, The Body Effect, Regions of Inversion: Approximate Limits, Strong Inversion, Weak Inversion, Moderate Inversion, A "Vnullnull Control" Point of View: Fundamentals, The "Pinchoff” Voltage. The Four-Terminal Mos Transistor: Transistor Regions of Operation, Complete All-Region Model, Simplified All-Region Models: Linearizing the Depletion Region Charge, Body-Referenced Simplified All-Region Models, Source-Referenced Simplified All-Region Models, Charge Formulation of Simplified All-Region Models, Models Based on Quasi-Fermi Potentials, Regions of Inversion in Terms of Terminal Voltages: Strong Inversion: Complete Strong-Inversion Model, Body-Referenced Simplified Strong-Inversion Model, Source-Referenced Simplified Strong-Inversion Model, Moderate-Inversion and Single-Piece Models, Source-Referenced vs. Body-Referenced Modelling , Effective Mobility, Effect of Extrinsic Source and Drain Series Resistances, Temperature Effects, Breakdown, The p-Channel MOS Transistor, Enhancement-Mode and Depletion-Mode Transistors, Model Parameter Values, Model Accuracy, and Model Comparison. | | | | 7 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | Small-Channel And Thin Oxide Effects: Carrier Velocity Saturation, Channel Length Modulation, Charge Sharing: Short-Channel Devices, Narrow-Channel Devices, Limitations of Charge-Sharing Models, Drain-Induced Barrier Lowering, Punchthrough, Hot Carrier Effects; Impact Ionization. Scaling: Classical Scaling, Modern Scaling. Large-Signal Modelling Of The Mos Transistor In Transient Operation: Quasi-Static Operation, Evaluation of Intrinsic Chargers in Quasi-Static Operation: Strong Inversion, Moderate Inversion, Weak Inversion, All-Region Model, Depletion and Accumulation.Transit Time under DC Conditions, Limitations of the Quasi-Static Model. Non-Quasi-Static Modelling: The Continuity Equation, Non-Quasi-Static Analysis. Extrinsic Parasitics: Extrinsic Capacitances, Extrinsic Resistance, Temperature Dependence, Simplified Models. | | | | 7 |
| **IV** | Small-Signal Modelling For Low And Medium Frequencies: Low-Frequency Small-Signal Model for the Intrinsic Part: Small-Signal Model for the Drain-to-Source Current, Small-Signal Model for the Gate and Body Currents, Complete Low-Frequency Small-Signal Model for the Intrinsic Part, Strong Inversion, Weak Inversion, Moderate Inversion, All-Region Models. A Medium-Frequency Small-Signal Model for the Intrinsic Part: Intrinsic Capacitances. Including the Extrinsic Part. Noise: White Noise, Flicker Noise, Noise in Extrinsic Resistances, Including Noise in Small-Signal Circuits. All-Region Models. Modelling For Circuit Simulation: Types of Models, Models for Device Analysis and Design, Device Models for Circuit Simulation, Attributes of Good Compact Models, Model Formulation: General Consideration and Choices. Common MOSFET Models Available in Circuit Simulators: BSIM, EKV, PSP, Other Models. | | | | 6 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. Yannis Tsividis and Colin McAndrew , “Operation and Modelling of the MOS Transistor”, 3/e, 2010. 2. T. Ytterdal, Y. Cheng and T. A. Fjeldly , “Device Modelling for Analog and RF CMOS Circuit Design”, John Wiley & Sons, 2003. 3. Narain Arora, “MOSFET ModellingFor VLSI Simulation: Theory And Practice”, World Scientific, 2007. | | | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 6077** | | RESEARCH METHODOLOGY | 1-1-0-2 | 2015 | |
| COURSE OBJECTIVES:   * To familiarize the students with different stages of research process. * To get an idea about descriptive and inferential statistics. * To familiarize the students with the nature of research and scientific writing.   **COURSE OUTCOMES:**   * The students should be able to understand the basic concepts of research and its methodologies. * Students are able to understand different statistical test and parameters. * The student should be able to define appropriate research problem and write a research report.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (18hrs) | | | | HRS |
| **I** | Introduction to research methodology. Types of research, research methods Vs methodology - stages of research process. Literature review – Problem definition- Research design for exploratory, descriptive and experimental research – Brief introduction to completely randomized design, randomized block design and Latin square designs (description only). | | | | 4 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | Sampling fundamentals -Types of sampling: probability and non-probability sampling. Sampling theory, sampling distribution and sample size determination. Tools and techniques of data collection: Questionnaire and schedule for field surveys, interview, observation, simulation, experimental and case study methods. Collection, recording, editing, coding and scaling of data. Scale classification and types. Measurement of validity, reliability and practicality. Cronbach’s Alpha. | | | | 5 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | Descriptive and inferential statistics - Data analysis and interpretation –testing of hypothesis, testing of population mean, variance and proportion –Z test – t test – F test - chi square test. Test for correlation and regression –standard error of the estimate. Testing goodness of fit. Brief introduction to non-parametric tests, factor analysis, discriminant analysis and path analysis (description only). Use of SPSS and other software. | | | | 4 |
| **IV** | Meaning of interpretation and inference: importance and care for interpreting results. Presentation of reports: popular reports and technical reports - structure and style. Oral and written presentations: Parts of a research report. Guidelines for writing research papers and reports – Writing different sections of a research paper – Introduction, Methodology, Results, Discussion, Conclusion, Abstract – Writing the title. Methods of giving references and appendices: referencing styles. Ethics in research. Use of computers and internet in research. | | | | 5 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. C. R. Kothari, "Research Methodology, Methods and techniques", New Age International Publishers, New Delhi, 2004. 2. R. Panneerseklvam, "Research Methodology", Prentice Hall of India, New Delhi, 2011. 3. Ranjit Kumar, "Research Methodology, A step by step approach", Pearson Publishers, New Delhi, 2005. 4. K. N. Krishnaswami, Appa Iyer and M Mathirajan, "Management Research Methodology", Pearson Education, Delhi, 2010. 5. M N Borse, "Hand Book of Research Methodology", Sree Nivas Publications, Jaipur, 2004. 6. William G Zikmund,"Business Research Methods", South – Western Ltd, 2003. 7. P K Majumdar, "Research Methods in Social Science", Viva Books Pvt Ltd, New Delhi, 2005. 8. Norman Blaikie, "Analyzing Quantitative Data", SAGE Publications , London, 2003 9. Samuel B. Green, Neil J. Salkind, "SPSS for Windows" Pearson Education New Delhi, 2007. | | | | | |
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| COURSE CODE | COURSE NAME | L-T-P-C | YEAR |
| **05EC 6091** | HDL LAB | 0-0-2-1 | 2015 |
| COURSE OBJECTIVES:   * To familiarize students with HDL. * To implement complex digital systems using FPGA.   **COURSE OUTCOMES:**   * Students will be able to take up and design advanced digital systems using FPGA. | | | |
| LIST OF EXERCISES / EXPERIMENTS (18hrs) | | | |
| a) Verilog/VHDL implementation and simulation of digital systems consisting of  1. Adder  2. Flip-flop  3. Counter  4. Comparator  5. Mux  6. Encoder  7. Shift registers  8. FSM  9. RAM  10. PWM  b) Hardware realization of FPGA based digital systems consisting of  1. ADC and DAC  2. UART Transceiver  3. VGA monitor  4. Microcontroller | | | |
| **INTERNAL TEST** | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 6002** | | MIXED SIGNAL VLSI DESIGN | 3-1-0-4 | 2015 | |
| COURSE OBJECTIVES:   * Device Modelling. * Various types of Analog systems. * CMOS amplifiers and Comparators.   **COURSE OUTCOMES:**   * Students will be able to apply the concepts of Analog design in various Analog systems including data converters, CMOS amplifiers, Comparators and Switched Capacitor Circuits.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (36hrs) | | | | HRS |
| **I** | Active Filters & Switched Capacitor Filters: Active filters: Active RC Filters for monolithic filer design: First & Second order filter realizations, universal active filter (KHN), self-tuned filter, programmable filters. Switched capacitor filters: Switched capacitor resistors, amplifiers, comparators, sample & hold circuits, Integrator-Biquad. | | | | 9 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | Continuous Time Filters & Digital Filters: Introduction to Gm-C filters: bipolar transconductors, CMOS transconductors using Triode transistors and active transistors, MOSFET C Filters (Tuning Circuitry, Dynamic range performance. Digital Filters: Sampling, decimation, interpolation, implementation of FIR and IIR filters. | | | | 9 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | Digital to Analog & Analog to Digital Converters: DAC: Non-idealities, types: Current switched, Resistive, Charge redistribution,Hybrid, segmented,Voltage Scaling, Cyclic, Pipeline,,Techniques for improving linearity. ADC: non-idealities,characteristics of Sample and Hold circuit, quantization errors,types:Flash, two step, pipelined, successive approximation, folding. | | | | 9 |
| **IV** | Sigma delta converters: Over sampled converters: Over sampling without noise & with noise, implementation imperfections, first order modulator, decimation filters, second order modulator, sigma delta DAC & ADC’s. | | | | 9 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. David A Johns and Ken Martin, “Analog Integrated Circuit Design”, John Wiley and Sons, 2002. 2. Rudy van de Plassche “Integrated Analog-to-Digital and Digital-to-Analog Converters”, Kluwer, 1999. 3. Antoniou, “Digital Filters Analysis and Design”, Tata McGraw Hill, 1998. 4. Phillip Allen and Douglas Holberg “CMOS Analog Circuit Design”, Oxford University Press, 2000. 5. Benhard Razavi, “Data Converters”, Kluwer Publishers, 1999. 6. Jacob Bake R, Harry W Li, and David E Boyce “CMOS, Circuit Design Layout and Simulation”, Wiley- IEEE Press, 1st Edition Aug, 1997. 7. Tsividis Y P, “Mixed Analog and Digital VLSI Devices and Technology”, Mc-Graw Hill, 1996. 8. Vineetha P. Gejji "Analog and Mixed Mode Design", Prentice Hall, 1st Edition , 2011. 9. Jeya Gowri, "Analog and Mixed Mode Design", Sapna publishing House, 2011. | | | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 6004** | | SENSOR TECHNOLOGIES AND MEMS | 2-1-0-3 | 2015 | |
| COURSE OBJECTIVES:   * Basic principles and techniques of sensors. * Measurement techniques of various physical quantities. * Signal conditioning circuits and interfacing.   **COURSE OUTCOMES:**  At the end of the course the student will be able to   * Choose suitable sensor/transducer for a given physical variable. * Understand its principle and characteristics. * Design suitable signal conditioning circuits for sensor/transducers. * To design a complete measurement system.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (27hrs) | | | | HRS |
| **I** | Introduction: Measurement systems, Basic electronic measuring system, Transduction principles, Classification of transducers, General transducers characteristics, Criteria for transducer selection. Resistive Transducers: Principles of operation, construction, theory, advantages and disadvantages, applications of Potentiometers, strain gauges, (metallic and semi-conductor type), Resistance Thermometer, Thermistors. | | | | 7 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | Inductive Transducers: Types of Inductive transducer, Principles of operation, construction, Advantages & disadvantages and applications. Various variable Inductive Transducers, LVDT (Linear variable differential transformer). Capacitive Transducers: Types of capacitive transducer, Principles of operation, construction, theory, advantages and disadvantages and applications, of capacitive transducers based upon familiar equation of capacitance. Elastic Transducers: Spring bellows, diaphragm, bourdon tube – their special features and application. | | | | 7 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | Active Transducers: Principle of operation, construction, theory, advantages and disadvantages and applications of following transducers: Thermocouple, Piezo-electric transducer, Magneto-strictive transducer, Hall effect transducer, Photo-voltaic transducer and Electrochemical transducer. Optical transducers: photo-emissive, photo-conductive and Photo-voltaic cells, Digital Transducers: Optical encoder, Shaft encoder. Feedback fundamentals, introduction to Inverse transducer, proximity sensors Transducers for liquid level measurement, humidity, silicon and quartz sensors, fibre optic sensors. Smart sensors: Introduction, primary sensors, converters, copensation. Recent trends in sensor technology – film sensors, semiconductor IC technology, MEMS, Nano-sensors. | | | | 7 |
| **IV** | Signal Conditioning: Concept of signal conditioning, Introduction to AC/DC Bridges. Op-amp circuits used in instrumentation, Instrumentation amplifiers, isolation amplifiers, analogue-digital sampling, introduction to A/D and D/A conversion, signal filtering, averaging, correlation, Interference, grounding, and shielding. | | | | 6 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. Murty D V S, “Transducers & Instrumentation”, PHI, New Delhi, 2000. 2. Sawhney A K, “Electrical and Electronics Measurements and Instrumentation”, Dhanpat Rai and Sons, New Delhi, 2000. 3. Kalsi H S, "Electronic Instrumentation", Tata McGraw Hill, New Delhi, 4th Ed., 2001. 4. Patranabis D, “Sensors and Transducers”, PHI, New Delhi, 2003. 5. Doebelin Ernest O, "Measurement Systems: Application and Design", Tata McGraw Hill Ltd., New Delhi, 2004. | | | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 6006** | | EMBEDDED REAL TIME SYSTEMS | 2-1-0-3 | 2015 | |
| COURSE OBJECTIVES:   * Introduce the concept of operating systems and real time systems. * Introduce µC/OS-II and its internal structure.   **COURSE OUTCOMES:**  At the end of the course the student will be able   * To present the mathematical model of the system. * To develop real-time algorithm for task scheduling. * To understand the working of real-time operating systems and real-time database. * To work on design and development of protocols related to real-time communication.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (36hrs) | | | | HRS |
| **I** | Real Time System concepts: Introduction to real time embedded systems, foreground/background systems, critical sections, resources, multitasking, context switching, scheduling, re-entrancy, task priorities, mutual exclusion, semaphores, inter-task communications, interrupts. Kernel Structure: Introduction to µC/OS-II and its internal structure, tasks, task states, task control blocks, how µC/OS-II implements a ready list, task scheduling, the idle task, how to determine CPU usage, how µC/OS-II handles interrupts. | | | | 7 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | Task Management: µC/OS-II’s services to create a task, delete a task, check the size of a task’s stack, change a task’s priority, suspend and resume a task, and get information about a task. Time Management: suspension of a task’s execution until some user specified time expires, resume from suspension and set value of a 32-bit tick counter. | | | | 7 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | Inter task Communication and Synchronization: Communication between tasks and ISRs (Interrupt Service Routines) and share resources. Implementation of semaphores, message mailboxes and message queues. | | | | 7 |
| **IV** | Memory Management: dynamic memory allocation feature using fixed-sized memory, memory control blocks, Creating a partition, obtaining a memory block, returning an memory block, Status of memory partition, using memory partition. | | | | 6 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. Jean J. Labrosse, “µC/OS-II, The Real-Time Kernel”. 2. Labrosse, Jean J. "µC/OS, The Real-Time Kernel" R & D Publications, 1992. 3. Allworth, Steve T. "Introduction To Real-Time Software Design", Springer-Verlag, 1981. 4. Comer, Douglas, "Operating System Design, The XINU Approach" , Prentice-Hall, Inc., 1984. 5. Deitel, Harvey M. and Michael S. Kogan, "The Design Of OS/2Reading", Addison-Wesley Publishing Company, 1992. 6. Ganssle, Jack G. “The Art of Programming Embedded Systems”, Academic Press, Inc., 1992. 7. Halang, Wolfgang A. and Alexander D. Stoyenko, "Constructing Predictable Real Time Systems", Kluwer Academic Publishers Group, 1991.   **WEB**  1.www.uCOS-II.com | | | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 6022** | | DESIGN OF POWER CONVERTERS (ELECTIVE 2) | 2-1-0-3 | 2015 | |
| COURSE OBJECTIVES:   * To understand the fundamentals of DC to DC switching regulators, single phase and three phase inverters. * To design converters for the given specifications. * To apply closed loop control techniques to optimize the performance of DC to DC converters. * To acquire hands on experience by implementing converters for embedded systems.   **COURSE OUTCOMES:**   * After completing the course the students will be able to design and implement different types of DC to DC converters and characterize the performance.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (27hrs) | | | | HRS |
| **I** | Linear series and shunt regulators, Non-isolated DC-DC converters: Single pole double throw switch, chopper, DC steady state, buck, boost, buck-boost converter, steady state analysis, effect of non-idealities, selection of power devices, continuous and discontinuous conduction modes. Isolated converters: forward converter, demagnetizing winding, dual switch forward converter, push-pull converter, half-bridge converter, full-bridge converter, flyback converter, Cuk converter, soft switching in converters, zero-current and zero voltage switching. | | | | 7 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | Power diodes, reverse recovery, softness factors, Power MOSFETs, Structure, Regions of Operation, Switching Characteristics, Thermal Analysis and Design, Gate Drivers for Power Converters, Floating Supply, Level Shifting, Gate Driver Circuit Implementation, Isolated and Non-isolated Drivers, snubbers, fundamentals of magnetics, design of DC inductor, design of flyback, forward and current transformer. | | | | 7 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | PWM Control Techniques, Voltage-Mode, Current-Mode and Gated Oscillator Control, Requirement for Stability, stabilizing voltage mode buck converter, Venable's K-Factor method, Measurement of Closed Loop Response, current mode control, Slope Compensation, non-minimum-phase systems, converter impedance and system stability. | | | | 7 |
| **IV** | Single-phase Voltage Source Inverters, Half-bridge and full-bridge VSI, Carrier-based PWM, unipolar and bipolar PWM, selective harmonic elimination, Three-phase VSI, Sinusoidal PWM, square-wave operation, zero sequence injection, Space-vector based Modulating Techniques, Feedback Techniques in VSI, Linear Control of VSIs in a Rotating Frame, multilevel inverters, Diode-Clamped Multilevel Inverter, multilevel cascaded H-bridge inverter, Flying-Capacitor Multilevel Inverter. Micro Project: The Micro Project will involve the full design and implementation of a switching regulator. The design will be built using discrete power FETs, driver circuits, compensation circuits, and ramp generator. | | | | 6 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. Muhammad H. Rashid, "Power electronics handbook Third Edition", Elsevier, 2011. 2. Marty Brown, "Power Supply Cookbook Second Edition", Newnes, 2001. 3. Ron Lenk, "Practical design of power supplies", John Wiley & Sons, 2005. 4. Nihal Kularatna, "Power Electronics Design Handbook", Newnes,1998. 5. Sanjaya Maniktala, "Switching Power Supplies A to Z", Newnes, 2006. 6. Abraham I. Pressman, "Switching Power Supply Design Third Edition", McGraw-Hill, 2009. 7. L. Umanand, "Power electronics essentials and applications", Wiley India, 2009. 8. Ned Mohan, "First Course on Power Electronics and Drives", MNPERE, 2003. | | | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 6024** | | SYSTEM IDENTIFICATION AND SYSTEM SIMULATION (ELECTIVE 2) | 2-1-0-3 | 2015 | |
| COURSE OBJECTIVES:   * To get idea about systems and its models and the response of the systems. * To understand static system identification methods. * To understand dynamic system identification methods. * To get an idea about simulation of static and dynamic systems.   **COURSE OUTCOMES:**  At the end of the course the student will be able to   * Students can identify and simulate static and dynamic systems. The response of the systems can also be analysed.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (27hrs) | | | | HRS |
| **I** | Introduction: Systems and Models, Terminology, Basic Problems, Mathematical Models Properties, Structural Model Representations, System Identification Procedure, Time Invariant Linear Systems, Simulation and Prediction, Models of Linear Time Invariant Systems, Models for Time varying and Nonlinear Systems. Review of System Response Methods: Time Domain: Impulse Response Model Representation, Transfer Function Model Representation, Direct Impulse Response Identification, Direct Step Response Identification, Impulse Response Identification Using Step Responses, Frequency Transfer Function, Sine-wave Response, Identification. Frequency Response Methods: Empirical Transfer-function Identification, Empirical Transfer-function Estimate, Critical Point Identification, Impulse Response Identification Using Input–output Data, Discrete-time Delta Operator. | | | | 7 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | Time-invariant System Identification I: Static System Identification, Linear Static Systems: Linear Regression, Least-squares Estimation, Interpretation of Least-squares Method, Bias, Accuracy, Identifiability. Nonlinear Static Systems: Nonlinear Regression, Nonlinear Least-squares Estimation, Iterative Solutions, Accuracy, Model Reparameterization: Static Case, Maximum Likelihood Estimation. Case Studies for Electrical and Electronic Systems. | | | | 7 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | Time-invariant System Identification II: Dynamic System Identification: Linear Dynamic Systems: Transfer Function Models, Equation Error Identification, Output Error Identification, Prediction Error Identification , Model Structure Identification, Subspace Identification, Linear Parameter-varying Model Identification, Orthogonal Basis Functions. Case Studies for Electrical and Electronic Systems. | | | | 7 |
| **IV** | Simulation of Static and Dynamic Systems: Probability Models: Introduction to Probability Models, Discrete Probability Models, Continuous Probability Models, Stochastic Models: Markov Chains, Markov Processes, Linear Regression, Time Series. Simulation of Dynamic Models: Introduction to Simulation, Continuous-Time Models, Euler Method. Simulation of Probability Models: Monte Carlo Simulation, The Markov Property, Analytic Simulation. | | | | 6 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. Karel J. Keesman , “System Identification: An Introduction”, Springer, 2011. 2. Mark M. Meerschaert , “Mathematical Modelling ”, Academic Press, 2013. 3. Lennart Ljung, “System Identification: Theory for the User”, 2/e, Pearson Education, 1998. 4. Rik Pintelon, Johan Schoukens, “System Identification: A Frequency Domain Approach”, John Wiley & Sons, 2004. 5. Ján Mikleš, Miroslav Fikar, “Process Modelling, Identification, and Control”, Springer, 2007. | | | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 6026** | | VLSI PROCESS TECHNOLOGY (ELECTIVE 2) | 2-1-0-3 | 2015 | |
| COURSE OBJECTIVES:   * To understand the students about the various fabrication steps involved in VLSI chip process technology. * To get an idea about the precise lithographic development techniques and corrective measures as per the design of the chip. * To get an idea about the industrial fabrication process steps such as diffusion, deposition and finishing process of VLSI chip.   **COURSE OUTCOMES:**   * The students will get an overall idea about the different process steps involved in the fabrication of a VLSI chip. This will enable them to work in fabrication industry.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (27hrs) | | | | HRS |
| **I** | Overview And Materials: An Introduction to Microelectronic Fabrication, Moore’s Law, ITRS. Semiconductor Substrates. Hot Processing: Diffusion: Dopant diffusivities, channeling, Fick's 1st and 2nd law of diffusion, different dopant profile study, Electric field effects, Segregation, microscopic model, vacancy and interstitial dependence. Thermal Oxidation: Types of oxides, furnace design, Deal Grove Model – wet and dry oxidation, thin oxide growth (deviation from Deal Grove), Rapid Thermal Oxidation. | | | | 7 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | Deposition and Growth: Physical Deposition: Evaporation and Sputtering: DC, RF, plasma, Chemical Vapour Deposition, Epitaxial Growth: MBE, Growth Kinetics: ALD, MOCVD, LPCVD, APCVD, PECVD etc. Ion Implantation: Implantation Modelling , Electronic and nuclear stopping, Channeling, Damage Annealing, Transient enhanced diffusion (TED). | | | | 7 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | Pattern Transfer: Optical Lithography, Non optical Lithographic Techniques, Photoresists, Exposure: Systems: optics, advanced lithography techniques, Exposure Development, Enhancement techniques: proximity correction, phase shift masks. Etching: Isotropic / anisotropic, selectivity, Wet and dry etch. Reactive ion etching (RIE), Chemical-mechanical polishing (CMP). | | | | 7 |
| **IV** | Process Integration: Device Isolation, Contacts, and Metallization. CMOS Techniques, GaAs Technologies, Silicon Bipolar Technologies, MEMS. | | | | 6 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. S.A. Campbell "The Science and Engineering of Microelectronic Fabrication", 2/e, OUP, India, 2012. 2. J.D. Plummer, M.D. Deal, P.G. Griffin, "Silicon VLSI Technology", Pearson Education, 2001. 3. S.K. Ghandhi, "VLSI Fabrication Principles – Silicon and Gallium Arsenide", John Wiley and Sons. | | | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 6032** | | HIGH SPEED DIGITAL DESIGN (ELECTIVE 3) | 2-1-0-3 | 2015 | |
| COURSE OBJECTIVES:   * To teach high-speed design techniques for both of Analog and digital circuits. * To explain high-speed properties of logic gates. * To explain standard high-speed measurement techniques.   **COURSE OUTCOMES:**   * The students will get a thorough knowledge of high speed signal propagation in circuits and cables. * The students will be able to apply this knowledge to determine where signal integrity issues may arise and how to solve problems of poor digital signal integrity.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (27hrs) | | | | HRS |
| **I** | High Speed Digital Design Fundamentals: Frequency and time, Time and distance, Lumped vs distributed, four kinds of reactance- ordinary capacitance and inductance, mutual capacitance and inductance, Relation of mutual capacitance and mutual inductance to cross talk. High Speed properties of Logic gates: Power, Quicent vs active dissipation, Active power driving a capacitive load, Input power, Internal dissipation, drive circuit dissipation, Totem pole and open circuit speed, Sudden change in voltage and current. Packaging of Digital Systems: Integrated circuit packages, Wire and cable, Connectors. | | | | 7 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | Measurement Techniques; Rise time and bandwidth of oscilloscope probes, self-inductance of probe ground loop, Effects of probe load on a circuit, slowdown of a system clock, observing cross talk, measuring operating margin. Transmission Lines; Problems of point to point wiring, signal distortion, EMI, cross talk, ideal distortion less lossless transmission line, Electrical models of wires. | | | | 7 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | Transmission Lines at High frequency: Infinite uniform transmission line, Lossy transmission line, Low loss transmission line, RC transmission line, Skin effect, Mechanics of skin effect, Proximity effect, Dielectric loss, Effects of source and load impedance, Reflections of a transmission line, End termination, Source termination, Very short line. | | | | 7 |
| **IV** | Termination: end termination, Rise time, dc biasing, power dissipation, Source termination, Resistance value, Rise time, Power dissipation, Drive current, Middle terminators, Connectors – mutual, series and parasitic capacitance. Power system: Stable voltage reference, Uniform voltage distribution, resistance and inductance distribution wiring, series resistance and lead inductance of a capacitance Clock Distribution: schemes, Timing margin, Clock skew, delay adjustments, Clock jitter. | | | | 6 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. Howard Johnson, “High-Speed Digital Design: A Handbook of Black Magic”, Prentice Hall. 2. Masakazu Shoji, “High Speed Digital Circuits”, Addison Wesley Publishing Company. 3. Jan M, Rabaey, “Digital Integrated Circuits: A Design perspective”, Second Edition, 2003. 4. Dally W.S. & Poulton J.W., “Digital Systems Engineering”, Cambridge University Press. | | | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 6034** | | LOW POWER VLSI DESIGN (ELECTIVE 3) | 2-1-0-3 | 2015 | |
| COURSE OBJECTIVES:   * To study the concepts on different levels of power estimation and optimization techniques.   **COURSE OUTCOMES:**   * The students will be able to design chips used for battery-powered systems and high-performance circuits not exceeding power limits.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (27hrs) | | | | HRS |
| **I** | Introduction – Need for low power VLSI, charging and discharging capacitance, short term current in CMOS circuit, CMOS leakage current, static current, basis principles of low power design, low power figure of merit. Physics of Power Dissipation MOSFET Devices –power dissipation in CMOS, low power VLSI design limits. | | | | 7 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | Design and test of low voltage CMOS – Circuit design style, Non clocked logic, NMOS and pseudo NMOS logic, Differential Cascade Voltage Switch logic, pass transistor logic, Clocked logic family, Domino logic, Differential Current Switch Logic, Leakage current in deep sub micron transistors, Deep submicron device design issues, Minimizing short channel effect, Low voltage circuit design techniques. | | | | 7 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | Low power static RAM – organization of static RAM, MOS static RAM cell, Banked organization of SRAMs, Reducing swings on bit lines, reducing power in write driver circuits, reducing power in sense amplifier circuits. | | | | 7 |
| **IV** | Adiabatic switching – Adiabatic charging, Adiabatic amplification, one stage and two stage adiabatic buffer, fully adiabatic system, Adiabatic logic gates, fully adiabatic sequential circuits, partially adiabatic sequential circuits, stepwise charging, pulsed power supplies. | | | | 6 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. Kaushik Roy, Sharat C Prasad, "Low power CMOS VLSI circuit design", Wiley India. 2. Anatha P Chandrakasan, Robert W Brodersen, "Low power digital CMOS Design", Kluwer Academic. 3. Kiat Seng Yeo, Kaushik Roy, "Low voltage, low power VLSI sub systems", Tata Mcraw Hill. 4. Gray Yeap, "Practical low power digital VLSI design", Springer. | | | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 6036** | | NANOMATERIALS, STRUCTURES AND DEVICES (ELECTIVE 3) | 2-1-0-3 | 2015 | |
| COURSE OBJECTIVES:   * To introduce state of the art nanomaterials. * The behaviour of nanomaterials, quantum phenomena and the limitations of basic physical laws that are important at the nanometre length scale are introduced and developed. * The course will also cover the environmental, health and ethical implications of nanomaterials in society.   **COURSE OUTCOMES:**   * Students will have a good understanding on structure-property relationships in nanomaterials. * The students will have broader concepts of a technology, applicable to smaller length scales. * The students will be able to evaluate the relevance of nanotechnology devices in the current scenario**.**   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (27hrs) | | | | HRS |
| **I** | Definition of Technology node. MOS Scaling theory, Issues in scaling MOS transistors: Short channel effects, Description of a typical CMOS technology. Requirements for Non classical MOS transistor. MOS capacitor, Role of interface quality and related process techniques, Gate oxide thickness scaling trend, SiO2 vs High-k gate dielectrics. Integration issues of high-k. Interface states, bulk charge, band offset, stability, and reliability – QBD high field, possible candidates, CV and IV techniques. | | | | 7 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | Metal gate transistor: Motivation, requirements, Integration Issues. Transport in Nano MOSFET, velocity saturation, ballistic transport, injection velocity, velocity overshoot. SOI - PDSOI and FDSOI. Ultrathin body SOI - double gate transistors, integration issues. Vertical transistors - FinFET and Surround gate FET | | | | 7 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | Metal source/drain junctions - Properties of schotky junctions on Silicon, Germanium and compound semiconductors -Workfunction pinning. Germanium Nano MOSFETs : strain , quantization , Advantages of Germanium over Silicon , PMOS versus NMOS. Compound semiconductors - material properties, MESFETs Compound semiconductors MOSFETs in the context of channel quantization and strain , Hetero structure MOSFETs exploiting novel materials, strain, quantization. | | | | 7 |
| **IV** | Synthesis of Nanomaterials : CVD, Nucleation and Growth, ALD, Epitaxy, MBE Characterization techniques for nanomaterials: FTIR, XRD, AFM, SEM, TEM, EDAX etc Emerging nano materials : Nanotubes, nanorods and other nano structures, LB technique, Soft lithography etc. Microwave assisted synthesis, Self assembly etc. | | | | 6 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. Y. Taur and T. Ning , “Fundamentals of Modern VLSI Devices”, Cambridge University Press. 2. Plummer, Deal, Griffin , “Silicon VLSI Technology”, Pearson Education India. 3. Brundle, C.Richard; Evans, Charles A. Jr., Wilson, Shaun, “Encyclopedia of Materials Characterization”, Elsevier. 4. Daniel Ratner, “Nanotechnology: A Gentle Introduction to The Next Big Idea”, Pearson Education India, 2003. | | | | | |
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| COURSE CODE | COURSE NAME | L-T-P-C | YEAR |
| **05EC 6066** | SEMINAR II | 0-0-2-2 | 2015 |
| COURSE OBJECTIVES:   * To improve the professional competency and research aptitude. * To motive and energize talent. * To improve presentation skills.   **COURSE OUTCOMES:**   * After successful completion of the seminar presentation, the students will be able to analyse and present technological and research topics more effectively. | | | |
| Each student shall present a seminar on any topic of interest related to the courses offered in the M.Tech Programme. He / she shall select the topic based on the references from international journals of repute, preferably IEEE journals. They should get the paper approved by the Programme Co-ordinator / Faculty member in charge of the seminar. The students should undertake a detailed study on the topic and submit a report at the end of the semester. | | | |
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| COURSE CODE | COURSE NAME | L-T-P-C | YEAR |
| **05EC 6088** | MINI PROJECT | 0-0-4-2 | 2015 |
| COURSE OBJECTIVES:   * To improve professional competency, research aptitude and team work skills. * To motive and energize talent. * To develop an aptitude to deliver commitments and manage time and stress pressures.   **GUIDELINES:** | | | |
| A list of Mini Projects should be prepared by the faculty before the commencement of the semester. The specifications and time plan should be clearly defined. The students should select a Project from the specified list and it can be done individually or in a group of two. The same project should not be selected by more than one group. Hardware design and fabrication is mandatory for all the projects.  The sequence of tasks may be   1. Schematic design and simulation 2. PCB layout design 3. Software/Firmware design and simulation 4. System integration and demonstration 5. Mini project report preparation | | | |
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| COURSE CODE | COURSE NAME | L-T-P-C | YEAR |
| **05EC 6092** | EMBEDDED SYSTEMS LAB | 0-0-2-1 | 2015 |
| COURSE OBJECTIVES:   * Introduce different interfaces available in ARM microcontroller and DSP processor. * Experiments consisting of programming, simulation, debugging, embedding and testing.   **COURSE OUTCOMES:**   * Students will be able to design software and hardware components of an embedded system. | | | |
| LIST OF EXERCISES / EXPERIMENTS (18 hrs) | | | |
| Design and hardware realization of embedded systems consisting of   1. Direct Memory Access 2. PWM 3. QEP 4. Analog-to-digital converter 5. Digital-to-Analog converter 6. Controller area network 7. Serial peripheral interface 8. Inter-integrated circuit 9. USB 10. Ethernet 11. FIR and IIR Filters 12. Audio signal processing 13. SD Cards | | | |
| **INTERNAL TEST** | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 7041** | | ELECTROMAGNETIC COMPATIBILITY (ELECTIVE 4) | 2-1-0-3 | 2015 | |
| COURSE OBJECTIVES:   * To familiarize with the fundamentals of EMI / EMC related to electronic products and industry. * To design electronic circuits compatible with EMI standards.   **COURSE OUTCOMES:**   * At the end of the course the student will be able to analyse Real-world EMC design constraints and make appropriate tradeoffs to achieve the most cost-effective design that meets EMI standards.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (27hrs) | | | | HRS |
| **I** | Electromagnetic Compatibility (EMC): Designing for EMC, EMC regulations, typical noise path, methods of noise coupling, and methods of reducing interference in electronic system. Cabling of Electronic Systems-Capacitive coupling, effect of shield on capacitive coupling, inductive coupling, effect of shield on inductive coupling, effect of shield on magnetic coupling, magnetic coupling between shield and inner conductor, shielding to prevent magnetic radiation, shielding a receptor against magnetic fields, Inductive coupling-shielding properties of various cable configurations, coaxial cable versus shielded twisted pair, braided shields, ribbon cables. | | | | 7 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | Grounding and Shielding Safety grounds, signal grounds, single-point and multipoint-point ground systems, hybrid grounds, functional ground layout, practical low frequency grounding, hardware grounds, grounding of cable shields, ground loops, Common Mode Choke - shield grounding at high frequencies, guarded instruments. Near fields and far fields, characteristic and wave impedances, shielding effectiveness, absorption and reflection loss, shielding with magnetic material, apertures, conductive gaskets, conductive windows, conductive coating, grounding of shields. | | | | 7 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | Conducted Emissions- power line Impedance-Switched Mode Power supplies- Power line Filters- power supply Instability-Magnetic field Emissions System Design for EMC –PCB layout and stack up- General Printed Circuit Board Design considerations –PCB chassis and Ground connection, Return Path Discontinuities- PCB layer Stack up Electrostatic Discharge (ESD) - Static generation, human body model, static discharge, ESD protection in equipment design, Transient and Surge Protection Devices, software and ESD protection, ESD versus EMC, ESD Testing. | | | | 7 |
| **IV** | Digital circuit power distribution: power supply decoupling, transient power supply currents, transient load current, Fourier spectrum, decoupling capacitors, effective decoupling strategies, multiple decoupling capacitors, target impedance, embedded PCB capacitance, power supply isolation, the effect of decoupling on radiated emissions, decoupling capacitor selection, placement and mounting. PCB layout considerations: PCB-to-chassis ground connection, return path discontinuities, slots in ground/power planes, split ground/power planes, changing reference planes, ground fill, PCB layer stack up, one- and two-layer boards, multilayer boards, four-layer boards, six-layer boards, eight-layer boards, general PCB design procedure, mixed-signal PCB layout, split ground planes, micro-strip ground plane current distribution, analog and digital ground pins, mixed-signal power distribution. | | | | 6 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. Henry W.Ott, “Electromagnetic Compatibility Engineering”, Wiley Interscience, 2009. 2. Henry W.Ott, “Noise Reduction Techniques in Electronic Systems”, 2/e, Wiley Interscience. 3. Clayton R.Paul, “Introduction to Electromagnetic Compatibility”, 2/e 4. Sonia Ben Dhia, Mohamed Ramdani, Etienne Sicard, “Electromagnetic Compatibility of Integrated Circuits Techniques for low emission and susceptibility”, Springer, 2006 5. David Morgan, “A Handbook for EMC Testing and Measurement”, 1/e, IET Electrical Measurement Series. 6. Mark I. Montrose, “EMC and the printed circuit board”, John Wiley & Sons, 1998. 7. Howard W. Johnson and Martin Graham, “High speed digital design”, Prentice Hall, 1993. | | | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 7043** | | TESTING OF VLSI CIRCUITS (ELECTIVE 4) | 2-1-0-3 | 2015 | |
| COURSE OBJECTIVES:   * In the VLSI design industry, a significant portion of work force and resources are been deployed in the test and validation of VLSI designs. The complexity of multimillion transistor based VLSI design calls for special techniques for efficiently testing and validating the VLSI design across all possible input, supply, speed and process corners. This has given rise to systematic areas of study in the form of design for test, automatic test pattern generation and these have all become very important areas from both research as well as routine industrial practice point of view. The present course will introduce the student to the mathematical and scientific principles based on which systematic test can be carried out on multimillion transistor VLSI design.   **COURSE OUTCOMES:**   * The student who completes this course will be familiar with the principles used in the construction VLSI Design for Test (DFT) tools. The student will be able to adapt these to his specific industrial needs, also contribute to the development of more efficient tools from the fault overage and speed point of view.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (27hrs) | | | | HRS |
| **I** | Introduction-VLSI testing process and Test Equipment- why fault Modelling -Fault Modelling -Logic and Fault Simulation-glossary of Faults- single stuck-at-faults-functional equivalence-bridging faults. | | | | 7 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | Logic simulation-Modelling single states-algorithm for true value simulation-serial and parallel fault simulation-Testability Measures-Combinational Circuit Test Generation- Sequential Circuit Test Generation. | | | | 7 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | Design for testability – Digital DFT and Scan design, Built-in Self test- random logic BIST, and Boundary Scan standard. | | | | 7 |
| **IV** | Memory Test-delay test-IDDQ Test. DFT Fundamentals- ATPQ Fundamental-Scan Architecture and Technique. System Test- Embedded Core Test-Future Testing. | | | | 6 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. Viswani D Agarwal and Michael L Bushnell, “Essentials of Electronic Testing of Digital Memory and Mixed Signal VLSI Circuits”, Springer, 2000. 2. Alfred L Cronch, “Design for Test for Digital IC’s and Embedded Core system”, Prentice Hall, 1999. 3. Niraj Jha and Sanjeep K Gupta, “Testing of Digital Systems”, Cambridge University Press, 2003. 4. M. Abramovici, M A Breuer and A D Friedman, “Digital systems Testing and Testable Design”, IEEE Press, 1994. | | | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 7045** | | VLSI SIGNAL PROCESSING (ELECTIVE 4) | 2-1-0-3 | 2015 | |
| COURSE OBJECTIVES:   * Introduce students to the fundamentals of VLSI signal processing and expose them to examples of applications. * Design and optimize VLSI architectures for basic DSP algorithms. * Introduce VLSI design techniques in communications systems. * Introduce algorithm, architecture, and circuit design tradeoffs to jointly optimize for power, performance, and area.   **COURSE OUTCOMES:**   * Students will be able to apply VLSI design methodology for signal processing systems. * Students will be familiar with VLSI algorithms and architectures for DSP. * Hands on experience on VLSI algorithm transforms including retiming, pipelining and parallel processing, folding/unfolding, algebraic transforms, relaxed look-ahead transforms, and dynamic algorithm transforms. * The students will be familiar with systolic architectures for DSP. * The students will be familiar with asynchronous and wave pipelines, scaling and round-off noise issues and their impact on performance. * Be familiar with fault-tolerant signal processing. * Be familiar with outer receiver VLSI design techniques.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (27hrs) | | | | HRS |
| **I** | Representation of DSP algorithms. Iteration Bound: Loop Bound, Iteration Bound, LPM Algorithm for iteration bound computation, Iteration Bound for multirate data flow graphs. Pipelining and Parallel Processing: Introduction. | | | | 7 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | Timing Techniques: Retiming: introduction, properties, system inequalities, retiming techniques Unfolding: Introduction, algorithm, properties, critical path, sample period reduction. Systolic architecture design: Introduction, Design Methodologies, Design B1 and B2. | | | | 7 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | Arithmetic architecture: Bit level arithmetic architecture, parallel multipliers, bit serial multipliers, Canonic Singed digit arithmetic, distributed arithmetic. The CORDIC Algorithms: Rotations and pseudo rotations, Basic CORDIC iterations, CORDIC hardware, Generalized CORDIC. | | | | 7 |
| **IV** | Fast convolution algorithms: Cook Toom, Winograd, Parallel FIR filters: Fast FIR, Pipelining of recursive filters: Introduction, pipeline interleaving, parallel processing in IIR filters.Scaling and round off noise computation. | | | | 6 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. Keshab V Parhi, "VLSI Digital Signal Processing", Willey India. 2. Peter Pirsch, "Architecture for Digital Signal Processing", Wiley. 3. Magdy A Bayoumi, "VLSI design methodologies for DSP architecture". 4. B. Parhami, "Computer Arithmetic: Algorithms and Hardware Designs", 2nd edition, Oxford University Press, 2010. 5. Israel Koren, "Computer Arithmetic Algorithms", 2nd Edition, CRC Press, 2001. 6. M.D. Ercegovac and T. Lang, "Digital Arithmetic", Morgan Kaufmann Publishers, 2004. | | | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 7051** | | VLSI AND COMPUTER AIDED DESIGN (ELECTIVE 5) | 2-1-0-3 | 2015 | |
| COURSE OBJECTIVES:   * Introduce Computer Aided Design (CAD) tools in VLSI circuits. * To introduce the concepts of Placement, Partitioning, Floor planning and routing using VLSI CAD design tools.   **COURSE OUTCOMES:**   1. After completing this course, students are expected to have completed one of the important prerequisites for professionals in the area of VLSI design. 2. Able to design a circuit using CAD TOOL. 3. Will have knowledge in different Algorithms.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (27hrs) | | | | HRS |
| **I** | Introduction to VLSI Physical Design: Physical Design Automation, VLSI Design Cycle, New Trends in VLSI Design Cycles, Design Styles. VLSI Physical Design Automation: Physical Design, Physical Design Cycle, VLSI Design Automation. Layout Compaction: Design Rules, Symbolic Layout, Problem Formulation: Applications of Compaction, Informal Problem Formulation, Graph-theoretical Formulation, Maximum-distance Constraints. Algorithms for Constraint-graph Compaction: A Longest-path Algorithm for DAGs, The Longest Path in Graphs with Cycles, The Bellman-Ford Algorithm, Discussion: Shortest Paths, Longest Paths and Time Complexity. | | | | 7 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | Placement and Partitioning: Circuit Representation, Wire-length Estimation, Types of Placement Problem, Placement at Various levels, Design-Style Specific Placement, Placement Algorithms: Constructive Placement, Iterative Improvement. Partitioning: Circuit Partitioning, Hierarchical Partitioning, Partition Levels, Problem Formulation, Classification of Partitioning Algorithms The Kernighan-Lin Partitioning Algorithm. | | | | 7 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | Floorplanning: Floorplanning Concepts, Terminology and Floorplan Representation, Hierarchical Design, Deadspaces, Design-Style Specific Floorplanning Optimization Problems in Floorplanning, Slicing and Non-Slicing Floorplans Shape Functions and Floorplan Sizing. | | | | 7 |
| **IV** | Routing: Types of Local Routing Problems, Area Routing, Channel Routing: Channel Routing Models, The Vertical Constraint Graph, Horizontal Constraints and the Left-edge Algorithm, Channel Routing Algorithms. Global Routing: Standard-cell Layout, Building-block Layout and Channel Ordering, Algorithms for Global Routing: Taxonomy of VLSI Routers, Design-Style Specific Routing | | | | 6 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. Gerez, “Algorithms for VLSI Design Automation”, John Wiley & Sons, 2006. 2. N. Sherwani, “Algorithms for VLSI Physical Design Automation”, Kluwer Academic Publishers, 1999. 3. Sadiq M. Sait and H. Youssef, “VLSI Physical Design Automation: Theory and Practice”, World Scientific, 1999. 4. Charles J. Alpert; Dinesh P. Mehta; Sachin S, “Handbook of Algorithms for Physical Design Automation”, Sapatnekar Auerbach Publications, 2008. | | | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 7053** | | HARDWARE / SOFTWARE CO-DESIGN (ELECTIVE 5) | 2-1-0-3 | 2015 | |
| COURSE OBJECTIVES:   * To develop skills for taking best from software and hardware design methods to solve complex electronic design problem. * To familiarize tradeoffs between flexibility and performance. * To effectively use the sequential way of decomposition in time and the parallel way of decomposition with space using hardware.   **COURSE OUTCOMES:**   * After completing the course the students will be able to practice hardware software partitioning and scheduling during the design of complex digital systems.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (27hrs) | | | | HRS |
| **I** | The nature of hardware & software - Introducing Hardware/Software Codesign The Quest for Energy Efficiency The Driving Factors in Hardware/Software Codesign The Hardware–Software Codesign Space The Dualism of Hardware Design and Software Design More on Modelling Concurrency and Parallelism, Data Flow Modelling and Implementation- The Need for Concurrent Models: An Example Tokens, Analyzing Synchronous Data Flow Graphs Control Flow Modelling and the Limitations of Data Flow Models Software Implementation of Data Flow Hardware Implementation of Data Flow, Analysis of Control Flow and Data Flow- Data and Control Edges of a C Program, Implementing Data and Control Edges Contraction of the Control Flow Graph Construction of the Data Flow Graph Application: Translating C to Hardware Single-Assignment Programs. | | | | 7 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | The Design Space of Custom Architectures: Finite State Machine with Datapath(FSMD)-Cycle-Based Bit-Parallel Hardware, Hardware Modules, Finite State Machines, Finite State Machines with Datapath Simulation and Register Transfer Level(RTL) Synthesis of FSMD Proper FSMD. Greatest Common Divisor(GCD) in Verilog (GCD mapping in other languages not required) Microprogrammed Architectures-Limitations of Finite State Machines, Microprogrammed Control, Microinstruction Encoding, The Microprogrammed Datapath Implementing a Microprogrammed Machine Microprogram Interpreters Microprogram Pipelining - Picoblaze: A Contemporary Microprogram Controller. | | | | 7 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | General-Purpose Embedded Cores-Processors, The Reduced Instruction Set Computer (RISC) Pipeline, Program Organization, Analyzing the Quality of Compiled Code SystemOnChip-The System-on-Chip(SoC) Concept, Four Design Principles in SoC Architecture, Example: Portable Multimedia System | | | | 7 |
| **IV** | Hardware/Software Interfaces & Applications: On-Chip Busses-Connecting Hardware and Software On-Chip Bus Systems Bus Transfers Multimaster Bus Systems On-Chip Networks Hardware/Software Interfaces- The Hardware/ Software Interface, Synchronization Schemes, Memory-Mapped Interfaces(Gezel Modelling not required), Coprocessor Interfaces, Custom-Instruction Interfaces Trivium Crypto-Coprocessor- The trivium stream cipher algorithm Trivium for 8 bit platforms. | | | | 6 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. Patrick R Schmount, “A practical introduction to hardware/software Codesign”, Springer, 2010. 2. Jorgen Staunstrup and Wayne Wolf, “Hardware/Software Co-Design: Principles and Practice”, Springer. 3. Frank Vahid and Tony D. Givargis, “Embedded System Design: A Unified Hardware/Software Introduction”, 2000. 4. J. Banks, J. S. Carson II, B. L. Nelson, and D. M. Nicol, "Discrete-Event System Simulation", Prentice-Hall, 2001. 5. A. Jantsch, “Modelling Embedded Systems and SoCs - Concurrency and Time in Models of Computation”, Morgan Kaufmann, 2003. 6. S. A. Edwards, “Languages for Digital Embedded Systems", Kluwer Academic Publishers, 2000. | | | | | |
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| COURSE CODE | | COURSE NAME | L-T-P-C | YEAR | |
| **05EC 7055** | | EMBEDDED NETWORKING (ELECTIVE 5) | 2-1-0-3 | 2015 | |
| COURSE OBJECTIVES:   * Introduce buses used in embedded systems. * Introduce industrial grade communication interfaces used in embedded systems. * Connectivity between various systems like embedded systems and PC. * Connectivity to internet via wired and wireless communication channels.   **COURSE OUTCOMES:**   * The students will be able to implement different communication channels and its protocols with signalling inside the embedded systems and to the outside world.   **SYLLABUS** | | | | | |
| MODULE | COURSE CONTENT (27hrs) | | | | HRS |
| **I** | Embedded Networking Requirements: Introduction to Network for Embedded Systems, Introduction to buses and protocols for embedded networking: CAN Bus, I2C, SPI, USB, Ethernet protocol, TCP/IP Protocol, Internet connectivity over an Ethernet connection, Wireless - Bluetooth, ZigBee standard. | | | | 7 |
| **INTERNAL TEST 1(Module 1)** | | | | | |
| **II** | Controller Area Network : CAN Overview, Introduction, CAN 2.0b Standard (covering Physical Layer, Message Frame Formats, Bus Arbitration, Message Reception and Filtering, Error Management), Selecting a CAN Controller, CAN Development Tools, Evaluating system requirements choosing devices and tools, Configuring single devices, Overall network configuration, Network simulation, Network Commissioning, Advanced features and testing. | | | | 7 |
| **INTERNAL TEST 2(Module 2)** | | | | | |
| **III** | SPI : Introduction, Features, Modes of Operation , External Signal Description, Functional Description(Covering Master Mode, Slave Mode, Transmission Formats, Baud Rate Generation, Error Conditions, Low Power Mode Options) I2C : I2C-bus features, Modes of Operation - Standard-mode, Fast-mode ,Fast-mode plus, Ultra fast mode(covering the following topics - Signals and Logic levels, Start/Stop conditions, byte format, Acknowledge and Not-Acknowledge, Clock Synchronization, Arbitration, Clock Stretching, Addressing, Call Addresses, Reset, DeviceID),Applications of I2C bus protocol. | | | | 7 |
| **IV** | TCP/IP: TCP/IP: Introduction to TCP/IP: History, Architecture, Standards and Applications, TCP/IP Architecture: Layering, Protocol Overview, Routers & Topology, IP routing, TCP Architecture, UDP Architecture, Security Concepts. ZigBee: Introduction, Comparison with Bluetooth, Short range wireless networking classes, Zigbee & IEEE802.15.4 standard, Operating frequencies, data rate, interoperability, Device types, Topologies, Communication basics, Association and Disassociation, binding, Self-forming and self-healing characteristics, Networking Layer functions, ZigBee gateway, Zigbee Metaphor, Networking Examples - Home Automation. | | | | 6 |
| **END SEMESTER EXAM (All Modules)** | | | | | |
| **REFERENCES:**   1. Lyla B Das, “Embedded Systems-An Integrated Approach”, Pearson, 2012. 2. Olaf P Feiffer, Andrew Ayre & Christian Keyold, “Embedded Networking with CAN and CAN Open”, Embedded System Academy, 2005. 3. Marco Di Natale, Haibo Zeng, Paolo Giusto & Arakadeb Ghosal, “Understanding and Using the Controller Area Network” , Springer, 2012. 4. John Catsoulis, "Designing Embedded Hardware", O'Reilly Media, Inc., 2002. 5. Dr. Sidnie Feit, “TCP/IP : Architectures, Protocols and Implementations with IPv6 and IP Security”, Tata McGraw Hill, Second Edition, 2008. 6. Martin W. Murhammer, Orcun Atakan, Stefan Bretz,Larry R. Pugh, Kazunari Suzuki, David H. Wood, “TCP/IP Tutorial and Technical Overview”, International Technical Support Organization-IBM, Sixth Edition, October 1998. 7. Wayne Wolf, “Computers as Components: Principles of Embedded Computing System Design”, Morgan Kaufman Publishers, 2008.   **WEB**   1. NXP Semiconductors, “I2C-bus Specification and User Manual” , Rev. 5, October 2012. (Available at <http://www.nxp.com/documents/user_manual/UM10204.pdf>). 2. Motorola Inc., “S12SPIV3/D:SPI Block Guide V03.06”, Feb 2003, (Available at http://www.ee.nmt.edu/~teare/ee308l/datasheets/S12SPIV3.pdf). | | | | | |
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| COURSE CODE | COURSE NAME | L-T-P-C | YEAR |
| **05EC 7067** | SEMINAR II | 0-0-2-2 | 2015 |
| COURSE OBJECTIVES:   * To improve the professional competency and research aptitude. * To motive and energize talent. * To improve presentation skills.   **COURSE OUTCOMES:**   * After successful completion of the seminar presentation, the students will be able to analyse and present technological and research topics more effectively. | | | |
| Each student shall present a seminar on any topic of interest related to the courses offered in the M.Tech Programme. He / she shall select the topic based on the references from international journals of repute, preferably IEEE journals. They should get the paper approved by the Programme Co-ordinator / Faculty member in charge of the seminar. The students should undertake a detailed study on the topic and submit a report at the end of the semester. | | | |
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| COURSE CODE | COURSE NAME | L-T-P-C | YEAR |
| **05EC 7087** | PROJECT (PHASE 1) | 0-0-12-6 | 2015 |
| The Project aims at providing the candidates, with an opportunity to design and build complete systems or sub-systems in the area of specialization. This includes the analysis, design of hardware/software, construction of an apparatus/instrument and testing and evaluation of its performance. A report is to be submitted at the completion of the project. The project will be evaluated on the basis of (i) physical inspection of the project (ii) project report and (iii) oral examination.  Project work Phase 1 includes   1. Selection of the area of specialization. 2. Selection of the project title from the area of specialization. 3. Literature survey, analysis and simulation. 4. Division of the project to sub tasks and time plan. 5. Formulation of the expected outcomes.   COURSE OBJECTIVES:   * To improve professional competency, research aptitude and team work skills. * To identify real world issues and develop innovative solutions. * To motive and energize talent. * To develop an aptitude to deliver commitments and manage time and stress pressures.   GUIDELINES:   1. Projects can be done individually, or in teams of two students. For a two-person group, group members are responsible for dividing up the work equally and making sure that each member contributes. 2. At least 50% should be continuing Projects so that it will evolve to an industry acceptance level. 3. Students in the first and second semester also should be associated with the Project work so as to improve continuity. 4. The groups are encouraged to come up with original ideas and novel real world applications for the projects. 5. The projects should involve well-designed experiments and thorough analysis of the experimental results. 6. It is highly desirable to produce a Research Paper and Patents based on the Project work. | | | |
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| COURSE CODE | COURSE NAME | L-T-P-C | YEAR |
| **05EC 7088** | PROJECT (PHASE 2) | 0-0-21-12 | 2015 |
| Phase 2 of the Project is the continuation of the work done in Project -Phase 1 which includes   1. Making necessary changes in the specifications and experimental methods based on the suggestions by the expert committee. 2. Detailed design. 3. Simulation and experimental works to realize the specifications of the project. 4. Result Analysis and Conclusion. 5. Preparation of the Project Report.   COURSE OBJECTIVES:   * To improve the professional competency, research aptitude and team work skills. * To identify real world issues and develop innovative solutions. * To motive and energize talent. * To develop an aptitude to deliver commitments and manage time and stress pressures. | | | |
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